



Title: GENERATING ADJUSTABLE-DELAY CLOCK SIGNAL FOR PROCESSING COLOR SIGNALS
Inventor: Ha Chu Vu
Docket No.: 08211/0200375-US0

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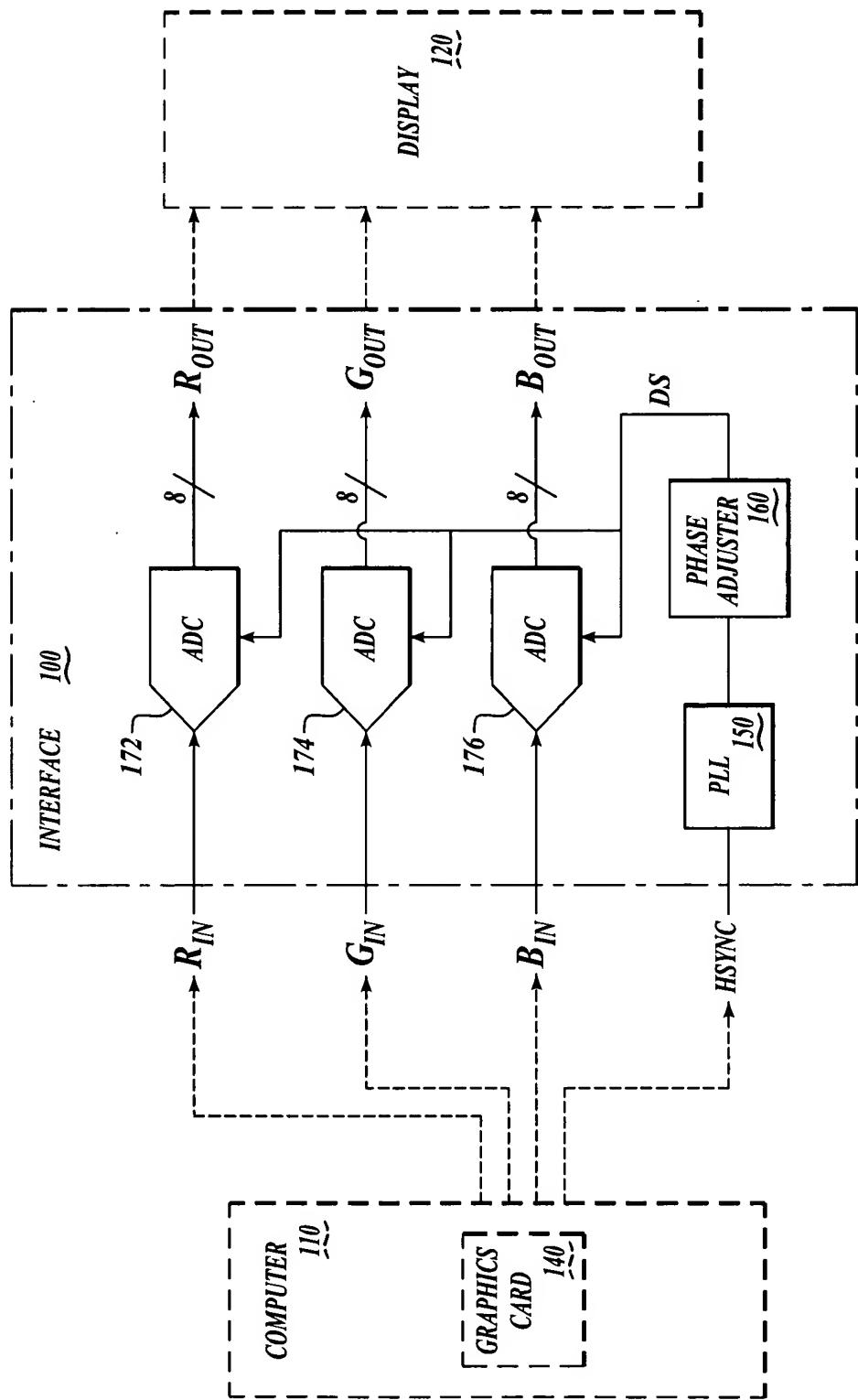


Fig. 1

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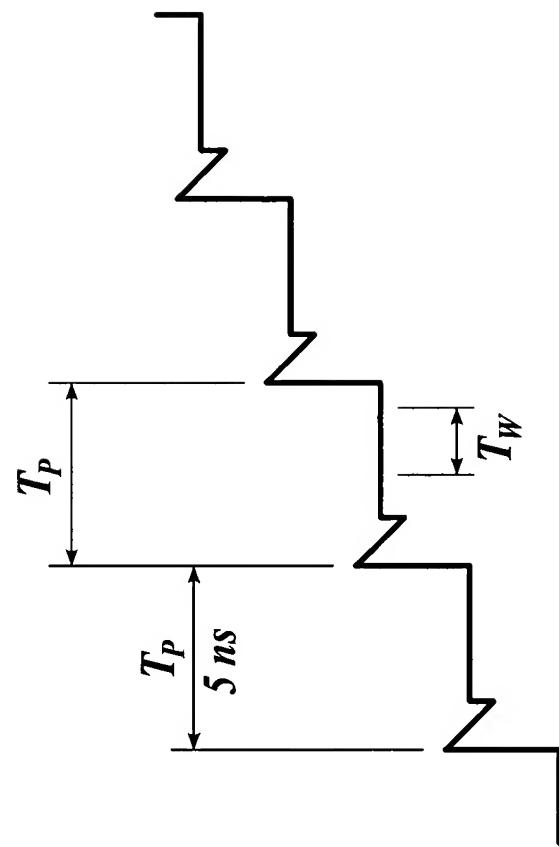


Fig. 2

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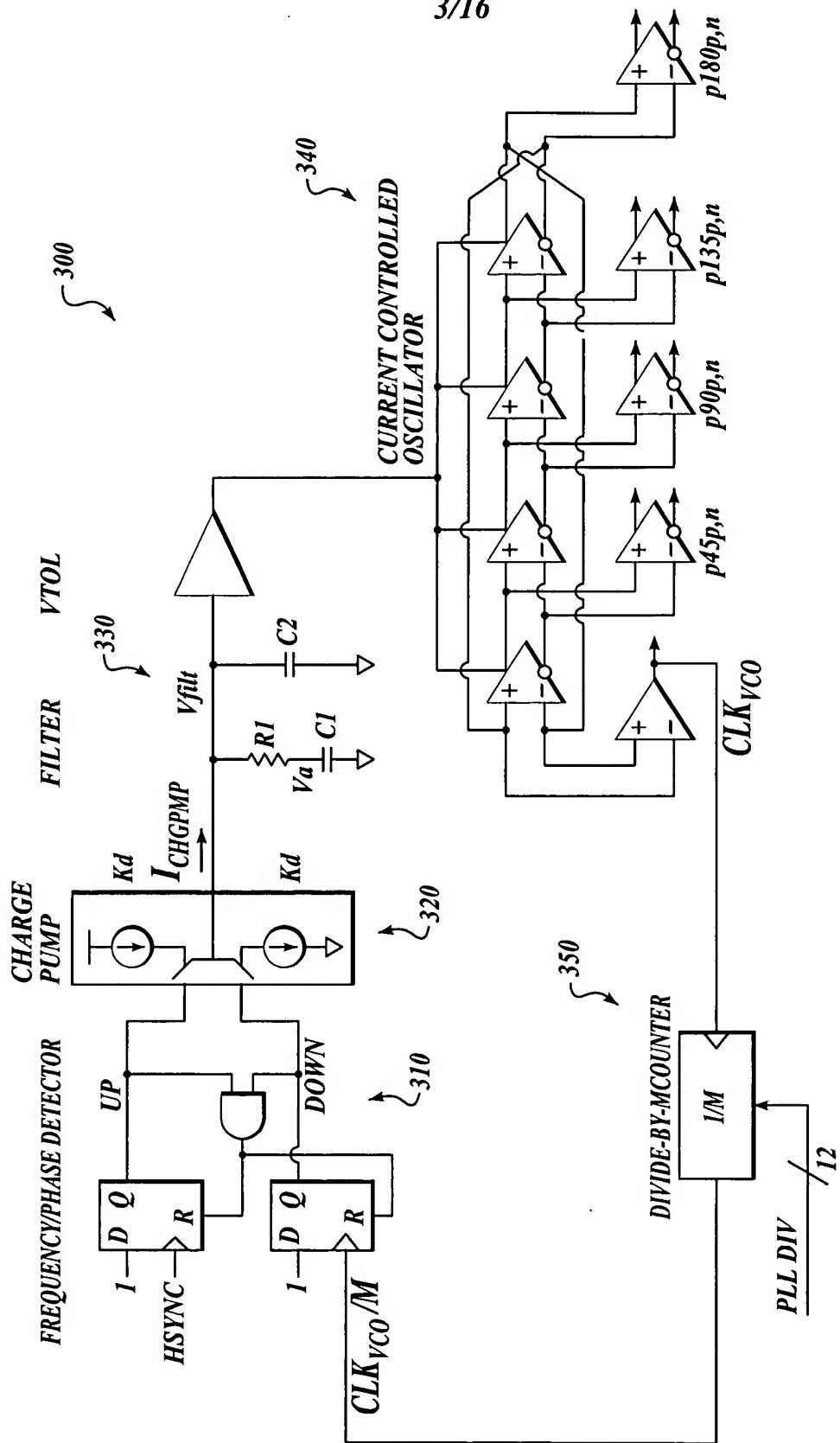


Fig. 3

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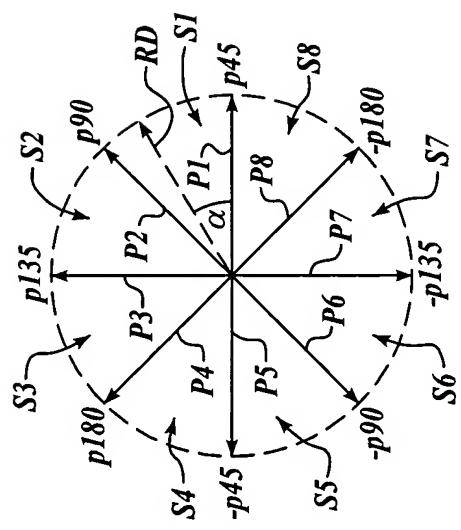
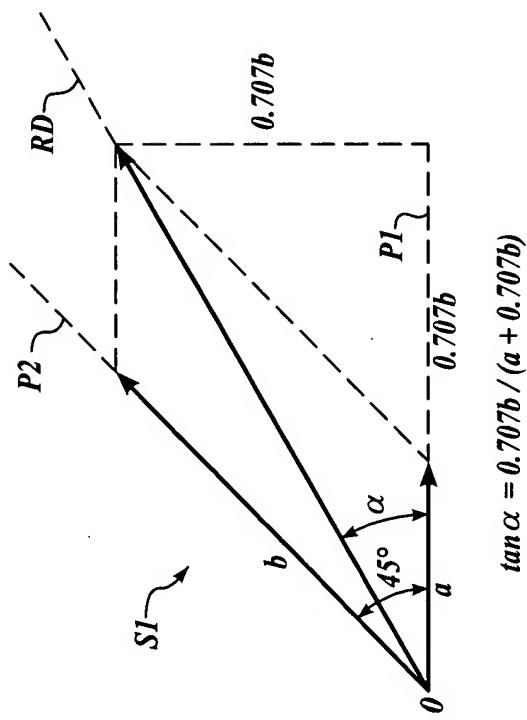


Fig. 4



$$\tan \alpha = 0.707b / (a + 0.707b)$$

Fig. 5

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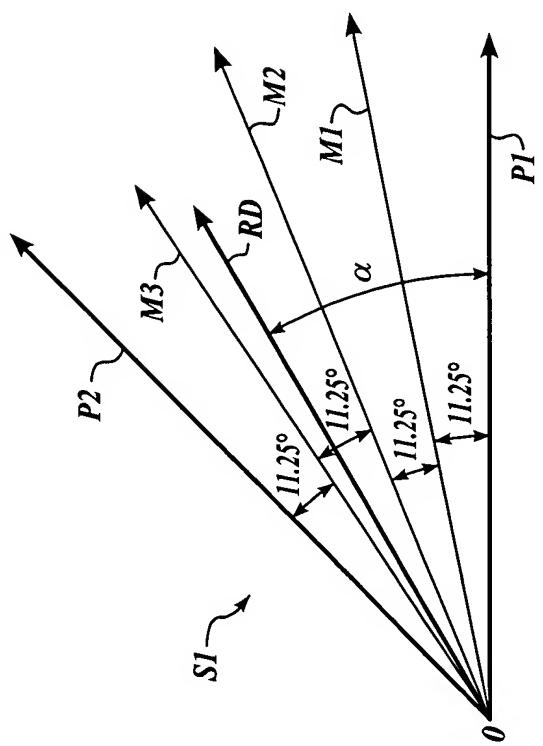


Fig. 6

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PHASE	α DEG.	SIMULATED		SET 1		SET 2	
		a	b	a	b	a	b
P1	0	16	0	4	0		
M1	11.25	12	4	3	1		
M2	22.5	8	8	2	2		
M3	33.75	4	12	1	3		
P2	45	0	16	0	4		

$TOTAL1 = 16$ $TOTAL2 = 4$

PHASE STEP = $360^\circ/32 = 11.25^\circ$
 $45^\circ/4 = 11.25^\circ$

WEIGHT VALUES FOR SIMULATED PHASES

Fig. 7

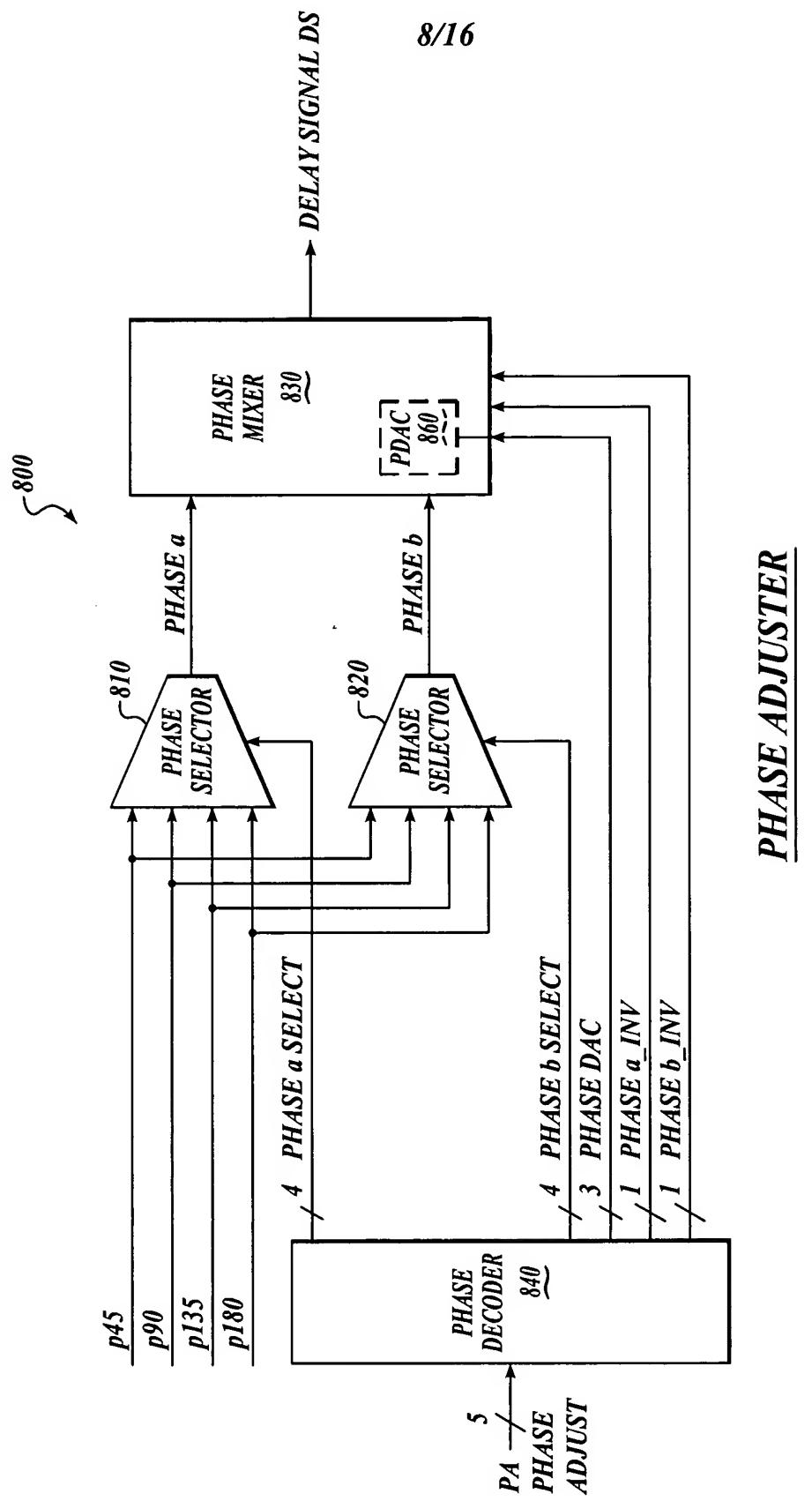


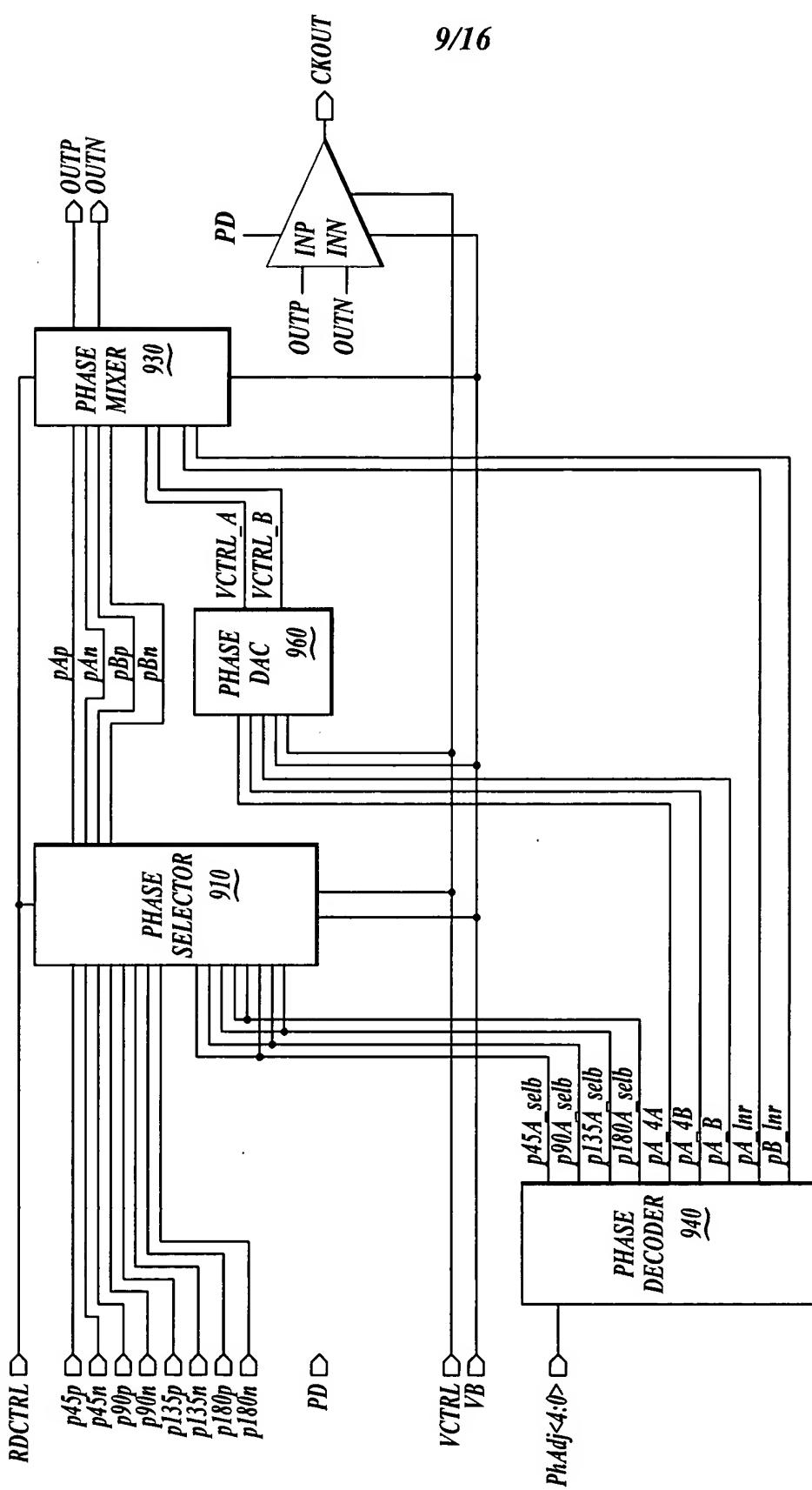
Fig. 8

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PHASE ADJUSTER IC

Fig. 9

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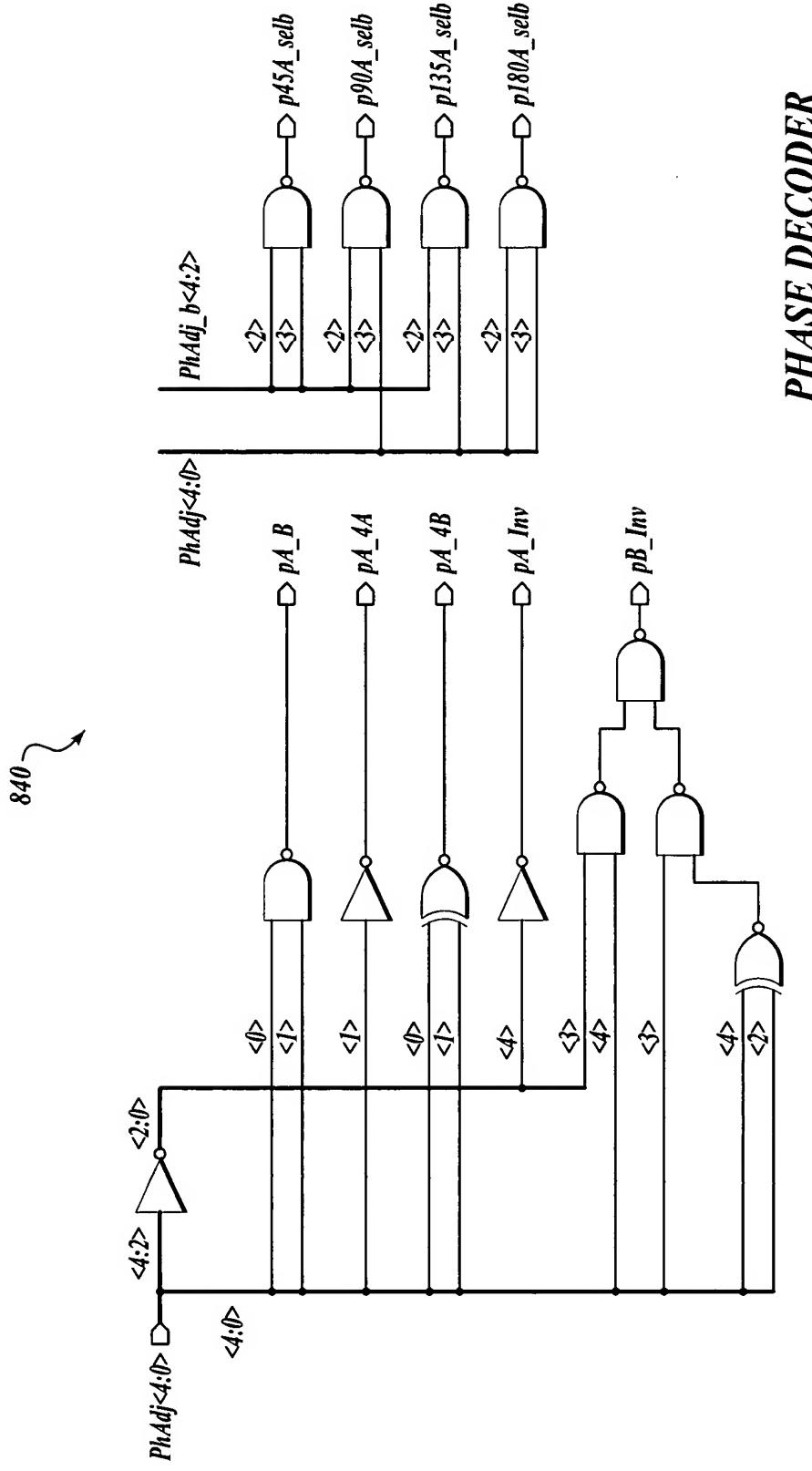


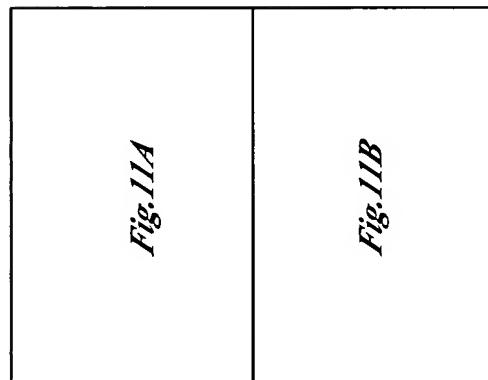
Fig. 10

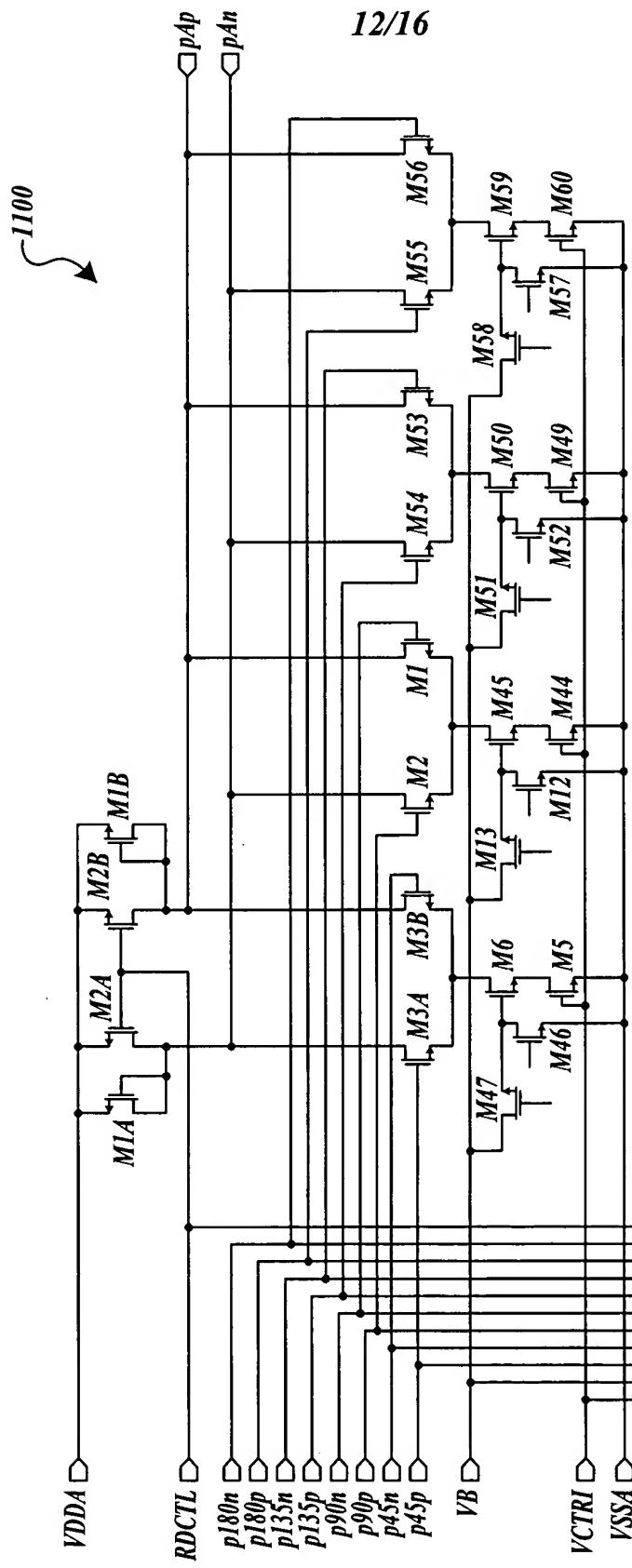
$VDDA \supset$
 $VSSA \supset$

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Fig. 11





PHASE SELECTOR CHIP

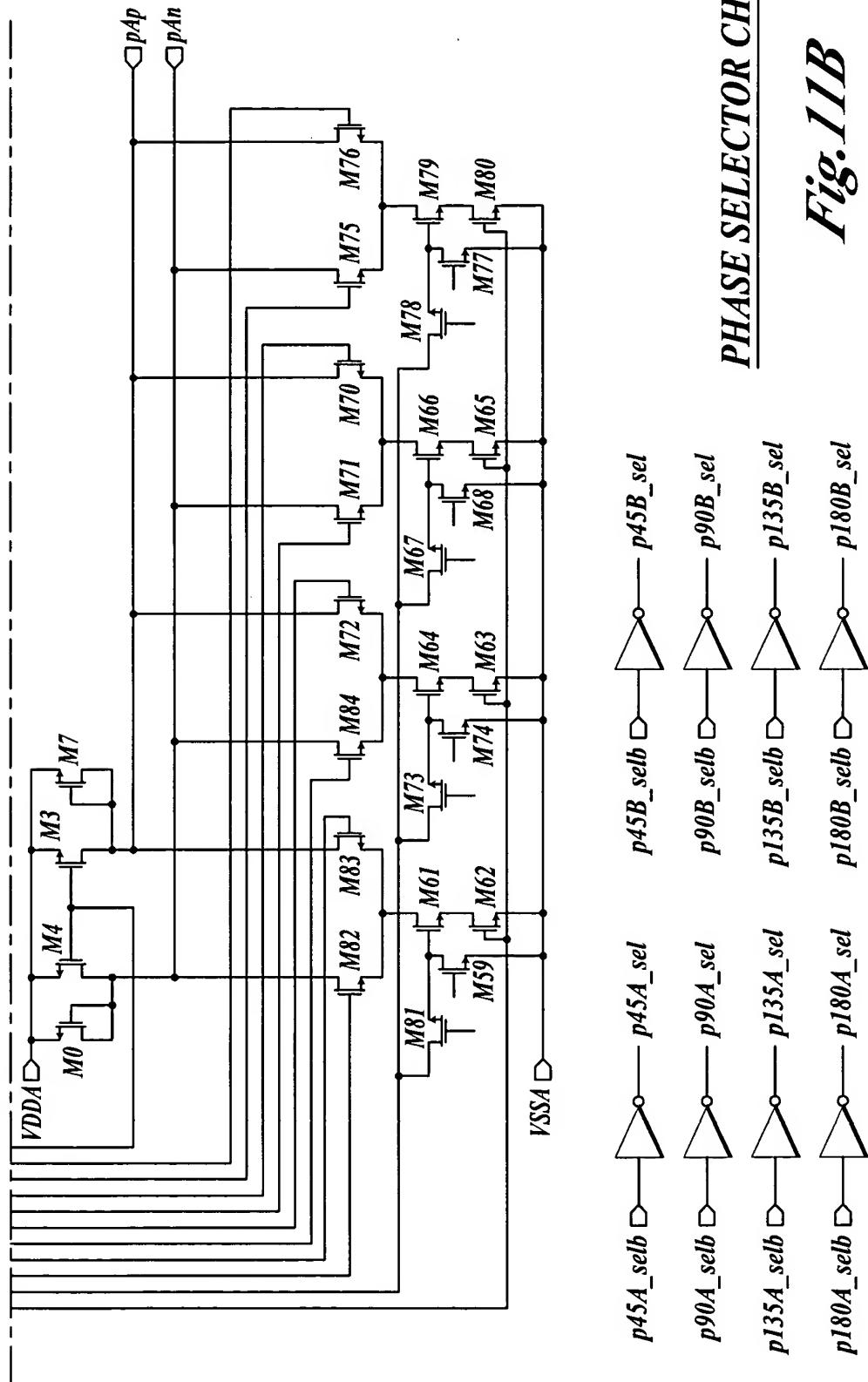
Fig. 11A

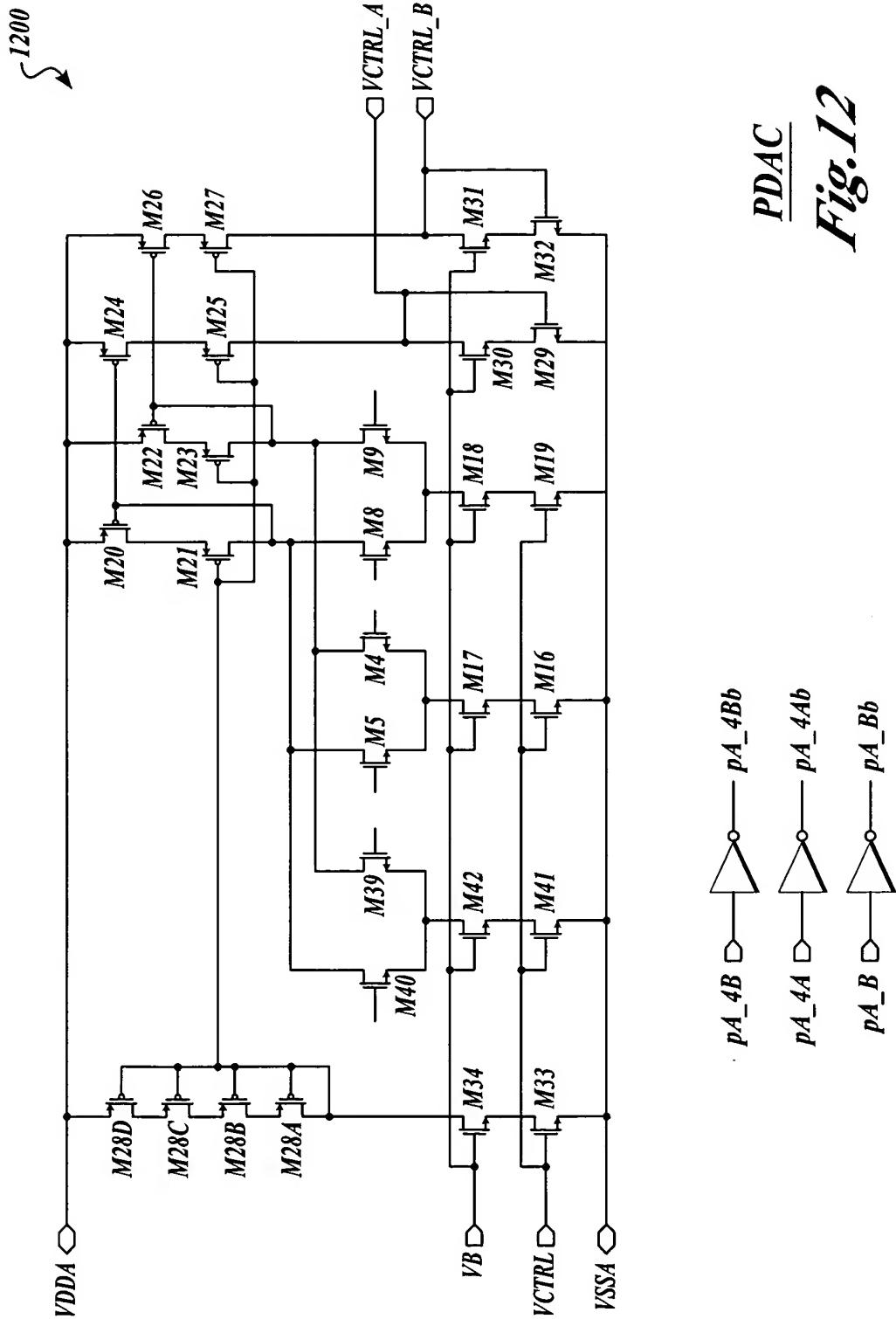
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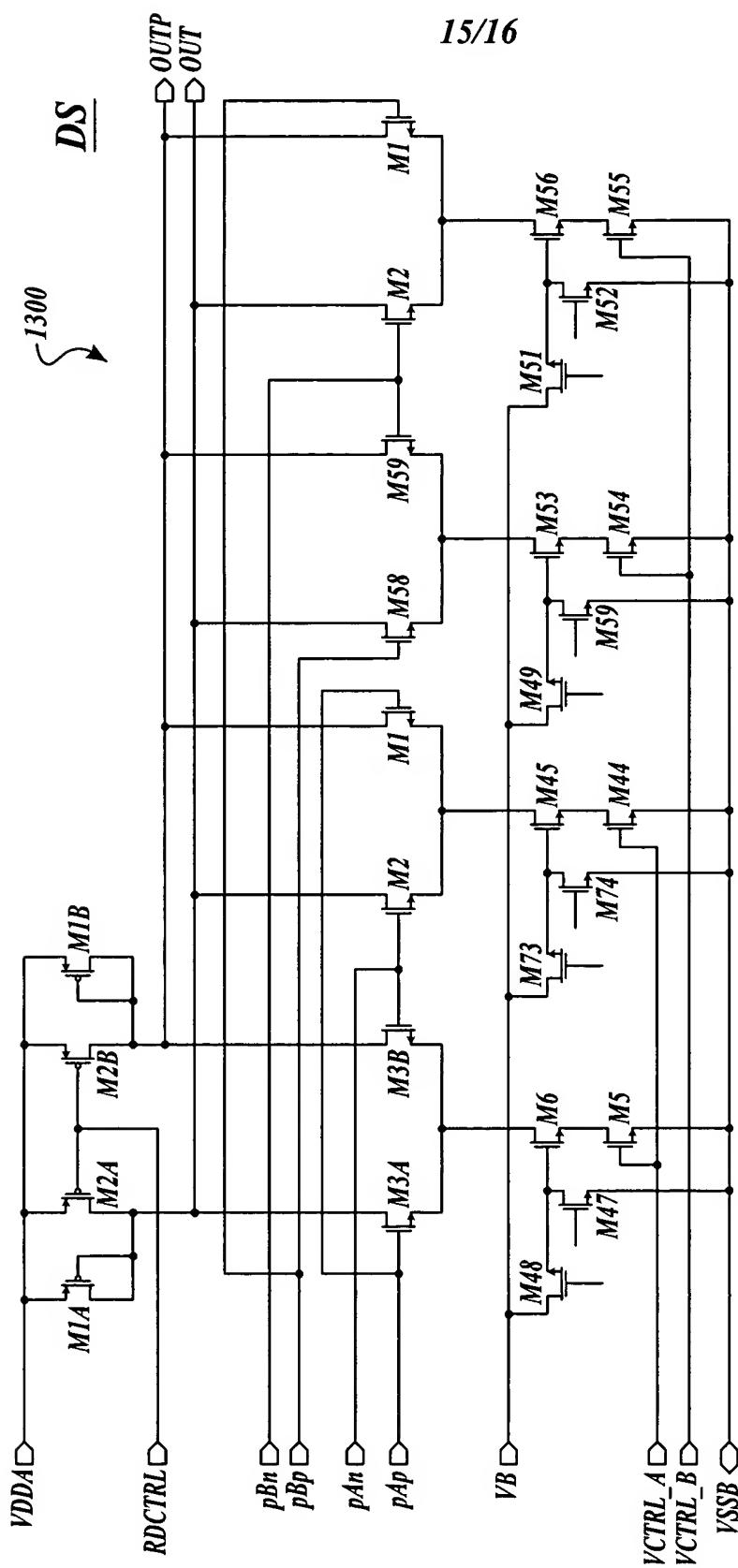


Fig. 13

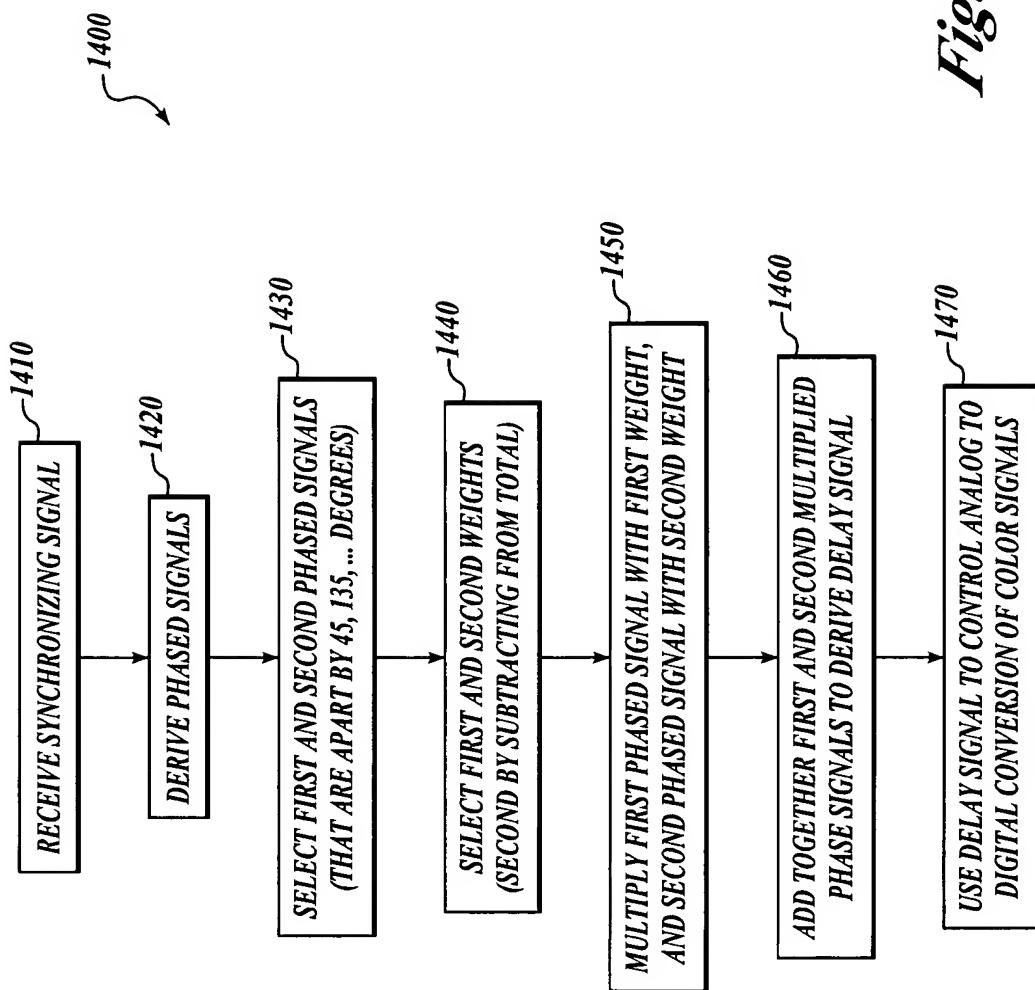


Fig. 14